

EXPERIMENT NO: 14

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Aim of the Experiment:

Analysis of JK Flipflop using eSim.

Theory:

This simple JK flip Flop is the most widely used of all the flip-flop designs and is considered to be a universal flip flop circuit. The JK flip flop is basically a gated SR Flip-flop S-R flip flop with the addition of a clock input circuitry. It prevents the invalid output condition that can occur when both inputs S and R are equal to logic level 1. Due to this additional clocked input, a JK flip-flop has four possible input combinations, logic 1, logic 0, no change and toggle.

Procedure:

1. Create the schematic of the JK Flipflop as shown in Figure-1.
2. Annotate the schematic.
3. Test Electric rules.
4. Generate the netlist.
5. Insert analysis for transient analysis from 0 to 100 Sec with a step time of 10 Sec.
6. Insert Source Details.
7. Insert values for Ngspice Models.
8. Convert KiCad netlist to Ngspice netlist.
9. Simulate the Ngspice netlist using Ngspice simulator.

Source Parameters:

For DC Voltage Source (V1):

1. Enter Value for V1 - 5

Following are the Pulse input parameters for V2:

1. Enter Initial Value - 0
2. Enter Pulsed Value - 5
3. Enter Delay Time - 1m
4. Enter Rise Time - 1m
5. Enter Fall Time - 1m
6. Enter Pulse Width - 20
7. Enter Period - 40

For DC Voltage Source (V3):

1. Enter Value for V3 - 0

For DC Voltage Source (V4):

1. Enter Value for V4 - 0

For DC Voltage Source (V5):

1. Enter Value for V5 - 0

Schematic Diagram:

The circuit schematic of JK flip flop in eSim is as shown below:

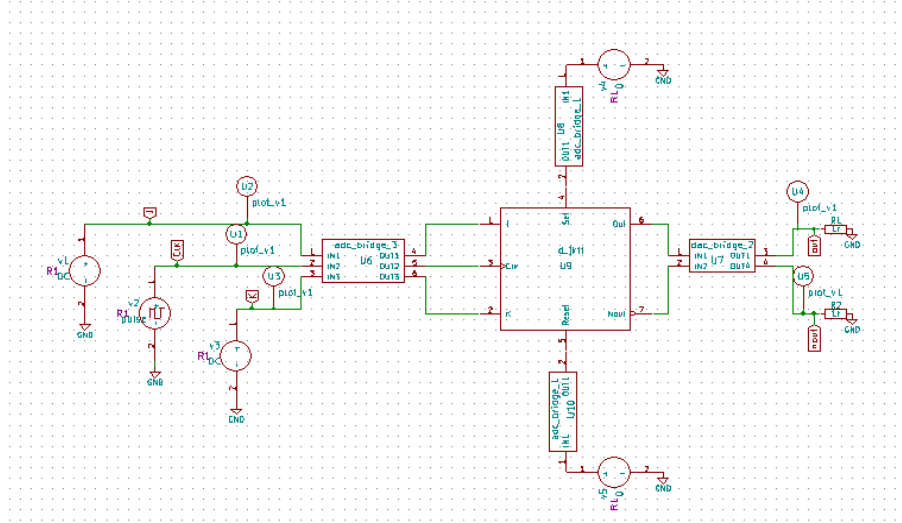


Figure 1: JK Flipflop

Simulation Results:

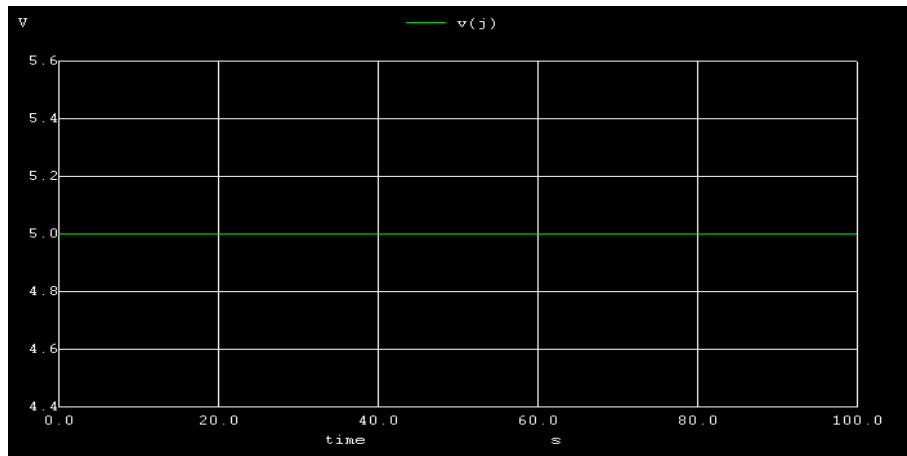


Figure 2: Ngspice Input-1 Plot

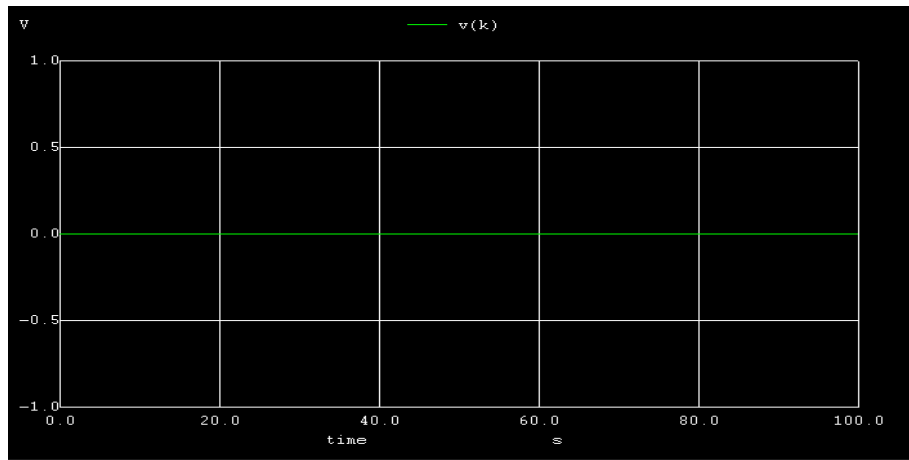


Figure 3: Ngspice Input-2 Plot

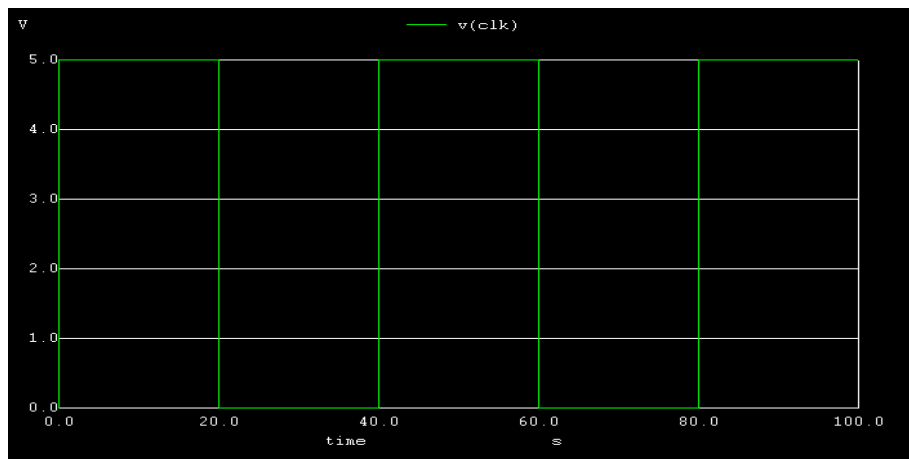


Figure 4: Ngspice Clock Input Plot

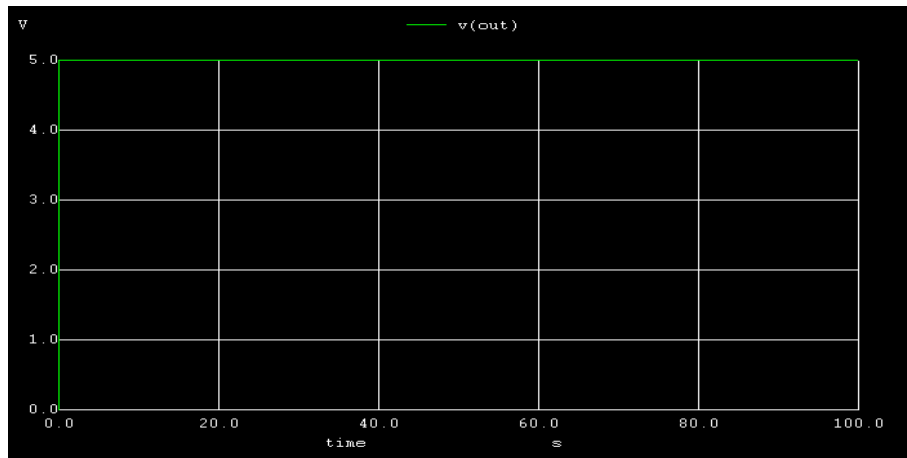


Figure 5: Ngspice Output-1 Plot

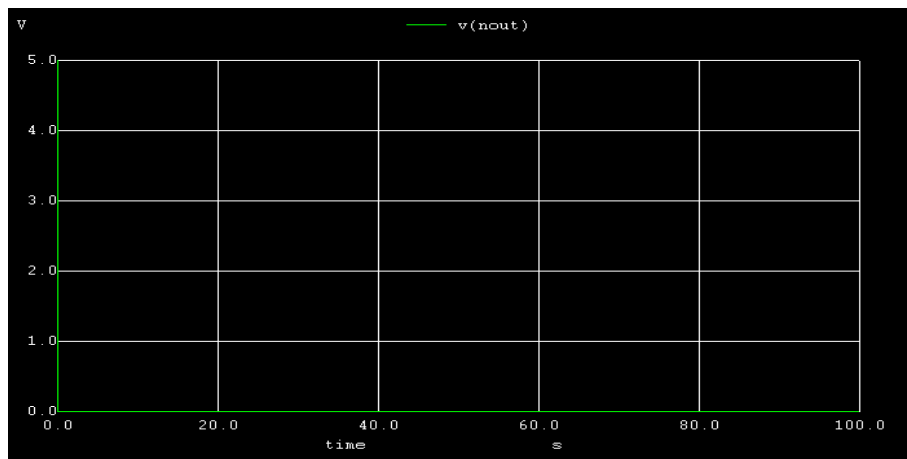


Figure 6: Ngspice Output-2 Plot

Conclusion:

Thus, we have studied the JK flip flop using eSim and we get the appropriate waveforms.

References:

<http://www.electronics-tutorials.ws/sequential/seq-2.html>